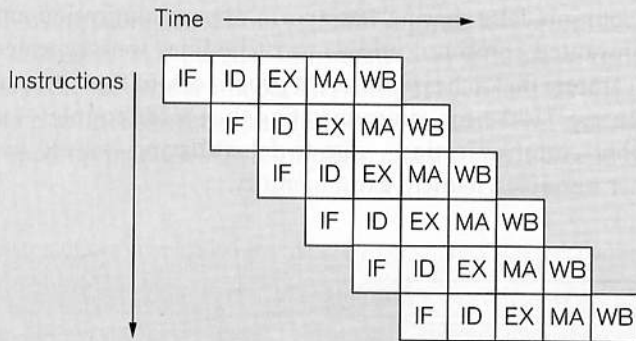


IF	ID	EX	MA	WB
IF Instruction fetch	ID Instruction decode/ register fetch	EX Execute	MA Memory access	WB Register write-back



**Figure 3.1**  
Simplified processor pipeline. By dividing instruction execution into five equal-size parts, five instructions can ideally be executing simultaneously, giving (ideally) a five-fold improvement over executing each individual instruction to completion.